WHAT IS CLAIMED IS:

1. A method comprising:

extracting, from a circuit description describing a circuit, information associated with circuit devices connected directly to an input of the circuit, wherein the extracted information includes information related to device connectivity and feature sizes;

aggregating the feature sizes of the circuit devices to obtain an aggregate feature size; and

determining a total capacitance of the input based, at least in part, on the aggregate feature size.

2. The method as in claim 1, further including:

extracting, from the circuit description, the information associated with circuit devices connected directly to each of a plurality of respective inputs and outputs; and

for each of the respective inputs and outputs:

aggregating the feature sizes of the circuit devices connected directly to the respective input or output to obtain an aggregate feature size; and

determining a total capacitance of the respective input or output based, at least in part, on the aggregate feature size.

3. The method as in claim 1, wherein determining the total capacitance includes determining a capacitance of a hypothetical feature having a feature size equivalent to the aggregate feature size.

4. The method as in claim 1, wherein the information associated with device connectivity includes information associated with wires connecting the circuit devices to the input, the method further including:

determining an aggregate capacitance of the wires; and

determining the total capacitance of the input based in part on the aggregate capacitance of the wires.

5. The method as in claim 1, further including providing the total capacitance of the input to a timing analysis tool.

6. The method as in claim 5 wherein the circuit description is a netlist.

7. The method as in claim 6, further including generating the netlist using a netlisting tool.

8. A method of making a computer readable medium product that encodes an integrated circuit design, the method comprising:

identifying substantially all inputs and outputs of a circuit;

extracting, from a circuit description, information associated with circuit devices connected directly to the respective inputs and outputs, wherein the information includes information related to device connectivity and feature sizes;

for each of the identified inputs and outputs:

aggregating the feature sizes of the circuit devices connected directly to the input or output to obtain an aggregate feature size; and

determining a total capacitance of the input or output based, at least in part, on the aggregate feature size;

generating an estimated timing response based on the total capacitance;

generating a circuit design using the estimated timing response; and

encoding the circuit design onto the computer readable medium product.

9. The computer readable medium product as in claim 8, wherein the information associated with device connectivity includes information associated with wires connecting the circuit devices to respective inputs and outputs, the method further comprises for each of the identified inputs and outputs:

determining an aggregate capacitance of the wires connected to the input or output; and

determining the total capacitance of the input or output based in part on the aggregate capacitance of the connected wires.

10. The computer readable medium product as in claim 8, wherein the computer readable medium is selected from the group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, an optically encodable disk, or a propagated signal.

11. A computer readable medium tangibly embodying a program of instructions, the program of instructions comprising:

at least one instruction executable to extract, from a circuit description describing a circuit, information associated with circuit devices connected directly to an input of the circuit, wherein the information includes information related to device connectivity and feature sizes;

at least one instruction executable to aggregate the feature sizes of the circuit devices to obtain an aggregate feature size; and

at least one instruction executable to determine a total capacitance of the input based, at least in part, on the aggregate feature size.

12. The computer readable medium as in claim 11, further including:

at least one instruction executable to extract, from the circuit description, the information associated with circuit devices connected directly to each of a plurality of respective inputs and outputs;

at least one instruction executable to aggregate the feature sizes of the circuit devices connected directly to each input or output to obtain an aggregate feature size for each input or output; and

at least one instruction executable to determine a total capacitance of each input or output based, at least in part, on the respective aggregate feature size.

13. The computer readable medium as in claim 11, wherein the at least one instruction executable to determine the total capacitance includes at least one instruction executable to determine a capacitance of a hypothetical feature having a feature size equivalent to the aggregate feature size.

14. The computer readable medium as in claim 11, wherein the information associated with device connectivity includes information associated with wires connecting the circuit devices to the input, and wherein the program of instructions further includes:

at least one instruction executable to determine an aggregate capacitance of the wires; and

at least one instruction executable to determine the total capacitance of the input based in part on the aggregate capacitance of the wires.

15. The computer readable medium as in claim 11, wherein the program of instructions further includes at least one instruction executable to provide the total capacitance of the input to a timing analysis tool.

16. The computer readable medium as in claim 11, wherein the computer readable medium is selected from the group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, an optically encodable disk, or a propagated signal.

17. A method comprising:

identifying substantially all inputs and outputs of a circuit;

extracting, from a circuit description, information associated with circuit devices connected directly to the respective inputs and outputs, wherein the information includes information related to device connectivity and feature sizes;

for each of the identified inputs and outputs:

aggregating the feature sizes of the circuit devices connected directly to the input or output to obtain an aggregate feature size; and

determining a total capacitance of the input or output based, at least in part, on the aggregate feature size

18. The method as in claim 17, wherein the information associated with device connectivity includes information associated with wires connecting the circuit

devices to respective inputs and outputs, the method further comprising for each of the identified inputs and outputs:

determining an aggregate capacitance of the wires connected to the input or output; and

determining the total capacitance of the input or output based in part on the aggregate capacitance of the connected wires.

19. The method as in claim 17, wherein determining the total capacitance includes determining a capacitance of a hypothetical feature having a feature size equivalent to the aggregate feature size.

20. The method as in claim 17, further comprising providing the total capacitance of each of the inputs and outputs to a timing analysis tool.

21. The method as in claim 17 wherein the circuit description is a netlist.

22. The method as in claim 21, further including generating the netlist using a netlisting tool.

23. A system comprising:

means for extracting, from a circuit description describing a circuit, information associated with circuit devices connected directly to an input of the circuit, wherein the information includes information related to device connectivity and feature sizes;

means for aggregating the feature sizes of the circuit devices to obtain an aggregate feature size; and

means for determining a total capacitance of the input based, at least in part, on the aggregate feature size.

24. The system as in claim 23, wherein:

the extraction means is for extracting, from the circuit description, the information associated with circuit devices connected directly to each of a plurality of respective inputs and outputs;

the aggregation means is for aggregating the feature sizes of the circuit devices connected directly to each of the plurality of inputs and outputs to obtain an aggregate feature size for each respective input and output; and

the determination means is for determining a total capacitance of each of the respective inputs and outputs based, at least in part, on the respective aggregate feature size.

25. The system as in claim 23, wherein the determination means includes hypothetical-feature means for determining a capacitance of a hypothetical feature having a feature size equivalent to the aggregate feature size.

26. The system as in claim 23, wherein the information associated with device connectivity includes information associated with wires connecting the circuit devices to the input and the system further includes:

wire aggregation means for determining an aggregate capacitance of the wires; and

wherein the determination means is for determining the total capacitance of the input based in part on the aggregate capacitance of the wires.

27. The system as in claim 23, further including providing means for providing the total capacitance of the input to a timing analysis tool.

28. The system as in claim 23, further including a means for generating the circuit description.